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10/673,211	09/30/2003	Xavier Montagne	003921.00136	9597

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,211	MONTAGNE ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' request for reconsideration filed on 02/21/2007 has been reviewed.

2. Amendment filed on 02/21/2007 has been entered.

3. Applicant's arguments filed on 02/21/2007 have been fully considered but they are not persuasive.

4. The applicants contend, "As per claim 1, there is no proper motivation or suggestion to combine Farooq with Herron."

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the examiner would like to point out that Farooq teaches a method for testing configurable logic blocks in an emulation system, the method comprising steps of: operating a first set to test a second set of configurable logic blocks (fig. 2, col. 3, lines 8-42, Farooq).

Herron et al. teach configuring a first set of configurable logic blocks to be first testing circuitry (fig. 9, 22, col. 3, lines 41-44, lines 62-66, col. 4, line 16, col. 14, lines 23-28, Herron et al.).

5. The applicants contend, "As per claims 7-8, the Action again fails to cite any portion of Farooq, Herron or Kattan as evidence of the motivation to combine the references."

The examiner disagrees and would like to point out that Kattan teaches a 37-bit counter 212 in the FPGA (col. 12, line 16, Kattan).

6. The applicants contend that claim 3 recites, among other features, "configuring a third set of configurable logic blocks to be second testing circuitry; and operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks." The combination of Farooq and Herron, even if proper, fails to teach or suggest at least this feature. In particular, the combination of references fails to teach concurrent operation of sets to test another set.

The examiner disagrees and would like to point out that Herron et al. teach configuring a third set of configurable logic blocks to be second testing circuitry (fig. 9, col. 3, lines 41-44, Herron et al.). Farooq teaches operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks (fig. 2, col. 2, lines 22-29, col. 3, lines 8-42, Farooq).

7. The applicants contend, "Again, even assuming, without admitting, that the combination of Butts and Cote does teach or suggest each and every feature of Applicants' claim 13 and 23, there is no proper motivation for combining the two references."

The examiner disagrees and would like to point out that Butts et al. teach that the present invention relates to the use of electronically reconfigurable gate array logic elements (ERCGAs), and more particularly relates to a methodology that includes interconnecting a plurality of such logic elements (col. 1, lines 11-15, Butts et al.).

Cote et al. teach that the invention relates more specifically to the problem of thoroughly and quickly testing large numbers and different types of interconnect resources such as those provided within an integrated circuit monolith that contains a programmable logic circuit such as a field programmable gate array (FPGA), col. 1, lines 12-17, Cote et al.

8. The applicants contend that as per claim 13 and 23, Butts fails to teach or suggest, "configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration."

The examiner disagrees and would like to point out that Butts et al. teach that an "interconnect chip" is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A "routing chip" is an interconnect chip used in a direct or channel-routing interconnect (col. 2, lines 15-19, Butts et al.). Thus implementing arbitrary interconnections among the I/O pins comprise inverse configuration.

9. The applicants contend, "Even assuming, without admitting, that the combination of Cote and Lesea does teach or suggest each and every feature of Applicants' claim 18, there is no proper motivation for combining the two references."

The examiner disagrees and would like to point out Cote et al. teach that the invention relates more specifically to the problem of thoroughly and quickly testing large numbers and different types of interconnect resources such as those provided within an integrated circuit monolith that contains a programmable logic circuit such as a field programmable gate array (FPGA), col. 1, lines 12-17, Cote et al.

Lesea teaches that in one embodiment, a field programmable gate array (FPGA) comprises a logic array, a data communication connection, and a serializer/deserializer circuit coupled to the data communication connection and the logic array. The logic array is programmable to perform test operations on the serializer/deserializer circuit (col. 2, lines 25-30, Lesea).

10. The applicants contend, "As per claim 18, Lesea does not describe that the first set is configured to provide a second test pattern to test the second test, and the second set is configured to output data in response to the second test pattern received from the first set."

The examiner disagrees and would like to point out Cote et al. teach that the first set is configured to provide a second test pattern to test the second test, and the second set is configured to output data in response to the second test pattern received from the first set (fig. 3B, 3C, 4A, 4B, col. 1, lines 10-13, col. 17, line 66 to col. 18, line 3, col. 23, lines 48-50, col. 24, lines 1-17, col. 25, lines 6-26, col. 25, lines 33-47, col. 26, lines 35-42, col. 27, lines 18-40, Cote et al.).

11. The applicants contend, "As per claim 18, Lesea does not describe "wherein the first set is further configured to provide an N-bit input generator to the second set and to provide a configurable logic block, separate from the N-bit input generator, as a verifier to verify the output data of the second set."

The examiner disagrees and would like to point out Cote et al. teach that each of each of LUT's 250, 260, 270 and 280 generates a respective, next-state output bit: Ao, Bo, Co, Do of the overall sequencer circuit (col. 11, lines 16-18, Cote et al.).

Lesea teaches that a field programmable gate array (FPGA) comprises input and output data communication connections, a serializer/deserializer circuit coupled to the input and output data communication connections, and a logic array programmed to generate a test data pattern coupled to the

output data connection. The logic array is further programmed to check a data pattern received on the input connection while performing a built in self test operation (fig. 2, col. 2, lines 34-42, Lesea).

12. The applicants contend, "As per claim 24, there is no proper motivation for combining Tseng and Cote references."

The examiner disagrees and would like to point out Tseng et al. teach that the FPGA chips include re-programmable means for configuring logic cells into the user-defined logic gates in response to configuration commands input to programming pins on the FPGA chips. Emulation I/O pins on the FPGA chips are coupled to the user-defined signals that are inputs and outputs of the logic cells of the FPGA chips configured as the user-defined logic gates (col. 2, lines 54-61, Tseng et al.).

Cote et al. teach that the invention relates more specifically to the problem of thoroughly and quickly testing large numbers and different types of interconnect resources such as those provided within an integrated circuit monolith that contains a programmable logic circuit such as a field programmable gate array (FPGA), col. 1, lines 12-17, Cote et al.

13. The applicants contend, "As per claim 24, Tseng et al. and Cote et al. fail to teach that wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set."

The examiner disagrees and would like to point out that Cote et al. teach that FIG. 3C shows another implementation... in the FPGA (fig. 3C, col. 25, lines 6-26, Cote et al.). Cote et al. also teach that it is within the contemplation of the invention to provide within computer-readable media (e.g., floppy diskettes, CD-ROM, DVD-ROM) and/or within manufactured and transmitted signals, FPGA-configuring bit streams in accordance with the above disclosure and/or to provide computer-understandable instructions to computers for causing the computers to perform automated stepping of FPGA's under-test through a battery of reconfigurations and test loops and readouts in accordance with the above disclosure (col. 27, lines 52-61, Cote et al.).

14. The applicants contend, "As per claim 25, there is no proper motivation for combining Tseng et al., Butts et al. and Cote et al. references."

The examiner disagrees and would like to point out Tseng et al. teach that the FPGA chips include re-programmable means for configuring logic cells into the user-defined logic gates in response to configuration commands input to programming pins on the FPGA chips. Emulation I/O pins on the FPGA chips are coupled to the user-defined signals that are inputs and outputs of the logic cells of the FPGA chips configured as the user-defined logic gates (col. 2, lines 54-61, Tseng et al.).

Butts et al. teach that the present invention relates to the use of electronically reconfigurable gate array logic elements (ERCGAs), and more particularly relates to a methodology that includes interconnecting a plurality of such logic elements (col. 1, lines 11-15, Butts et al.).

Cote et al. teach that the invention relates more specifically to the problem of thoroughly and quickly testing large numbers and different types of interconnect resources such as those provided within an integrated circuit monolith that contains a programmable logic circuit such as a field programmable gate array (FPGA), col. 1, lines 12-17, Cote et al.

15. The applicants contend that as per claim 25, none of the references teaches or suggests "wherein the second routing portion is configured to map N inputs of the second routing portion to N outputs of the second routing porting in a second manner inverse to the first manner."

The examiner disagrees and would like to point out that Butts et al. teach that an "interconnect chip" is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A "routing chip" is an interconnect chip used in a direct or channel-routing interconnect (col. 2, lines 15-19, Butts et al.). Thus implementing arbitrary interconnections among the I/O pins comprise inverse configuration.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claims 1, 2, 3, 4, 5, 6, 9, 10, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq (US 6,760,277 B1) in view of Herron et al. (US 6,996,758 B1). Please see the office action mailed on 11/27/2006 for details.

19. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq (US 6,760,277 B1) and Herron et al. (US 6,996,758 B1) as applied to claim 6 above, and further in view of Kattan (US 6,621,767 B1). Please see the office action mailed on 11/27/2006 for details.

20. Claims 13, 14, 15, 16, 17, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts et al. (US 5,036,473) in view of Cote et al. (US 6,470,485 B1). Please see the office action mailed on 11/27/2006 for details.

21. Claim 18, 19, 20, 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cote et al. (US 6,470,485 B1) in view of Lesea (US 6,874,107 B2). Please see the office action mailed on 11/27/2006 for details.

22. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Cote et al. (US 6,470,485 B1). Please see the office action mailed on 11/27/2006 for details.

23. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Butts et al. (US 5,036,473) and Cote et al. (US 6,470,485 B1). Please see the office action mailed on 11/27/2006 for details.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dipakkumar Gandhi
Patent Examiner

CYNTHIA BRITT
PRIMARY EXAMINER